SOURCE DRIVER INCLUDING OUTPUT BUFFER, DISPLAY DRIVING CIRCUIT, AND OPERATING METHOD OF SOURCE DRIVER

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority from Korean Patent Application No. 10-2015-0108147, filed on Jul. 30, 2015, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

BACKGROUND

[0002] 1. Field

[0003] The exemplary embodiments disclosed herein relate to a source driver, and more particularly, to a source driver including an output buffer, a display driving circuit, and an operating method of the source driver.

[0004] 2. Description of the Related Art

[0005] Flat panel displays are widely used in smartphones, laptop computers, monitors, and other electronic devices. For example, liquid crystal display (LCD), an organic electro-luminance display, and other types of displays are generally used as flat panel displays. Flat panel displays include a panel for realizing an image, and a plurality of pixels are disposed on the panel. The image is realized on the panel, as the pixels are driven according to a data signal provided by a display driver integrated circuit (IC).

[0006] In order to prevent deterioration of the pixels, a technology to drive a data line by a polarity reversal method has been proposed. The polarity reversal method may include, for example, a frame reversal method that reverses polarities in a frame unit, a line reversal method that reverses polarities in a line unit, and a dot inversion method that reverses polarities in a pixel unit. Along with this polarity reversal method, a charge sharing function which shares charges of data lines has been used to reduce power consumption and improve visibility.

[0007] In the charge sharing operation, a buffer output has to be prevented from being provided to data lines and the plurality of data lines have to be electrically connected, and thus, a plurality of switches have to be further included in the display driver IC. Such an increase in the number of switches may raise manufacturing costs and may increase a die area. Therefore, an efficient design of the display driver IC is required.

SUMMARY

[0008] The exemplary embodiments provide a source driver, a display driving circuit, and an operating method of the source driver, which have efficient designs and thereby reduce manufacturing costs and sizes.

[0009] According to an aspect of an exemplary embodiment, there is provided a source driver including: a buffer device including a plurality of buffers corresponding to a plurality of data lines, wherein each of the plurality of buffers respectively comprises an amplifier configured to amplify an input signal and an output driver configured to output a driving signal to a corresponding data line among the plurality of data lines; and a switch device comprising a charge sharing switch configured to electrically connect the plurality of data lines to one another during a charge sharing operation, wherein the amplifier comprises a first current

mirror having a reference current path comprising a first node and an output current path comprising a second node, and the first node of the reference current path and the second node of the output current path are electrically connected to each other during the charge sharing operation. [0010] The amplifier may further include a first switch connected between the first node and the second node, and the first switch may be turned on during the charge sharing operation.

[0011] The source driver may further include a control logic configured to generate a first control signal for disabling the output driver and a second control signal configured to turn on the first switch during the charge sharing operation.

[0012] The output driver may be disabled during the charge sharing operation.

[0013] The plurality of buffers may be provided in a path which negatively feeds back the driving signal from an output end to an input end of the plurality of buffers.

[0014] Voltage levels of the first node and voltage levels of the second node during the charge sharing operation may correspond to voltage levels of the plurality of buffers during a normal state.

[0015] The amplifier may further include a second current mirror having a reference current path comprising a third node and an output current path comprising a fourth node, and in the second current mirror, the third node of the reference current path and the fourth node of the output current path may be electrically connected to each other during the charge sharing operation.

[0016] The amplifier may further include a bias device, the reference current path may include a first transistor including a first gate and a second transistor including a second gate, the first transistor and the second transistor may be connected in series to each other between a first voltage and the bias device, the output current path may include a third transistor including a third gate and a fourth transistor including a fourth gate, the third transistor and the fourth transistor may be connected in series to each other between the first voltage and the bias device, and the first gate of the first transistor may be connected to the third gate of the third transistor, and the second gate of the second transistor may be connected to the fourth transistor.

[0017] The first node may be provided between the first transistor and the second transistor, and the second node may be provided between the third transistor and the fourth transistor.

[0018] The first node may be provided between the second transistor and the bias device, and the second node may be provided between the fourth transistor and the bias device.
[0019] The first node may be provided between the first transistor and the second transistor or between the second transistor and the bias device, and the second node may be provided between the third transistor and the fourth transistor or between the fourth transistor or between the fourth transistor and the bias device.

[0020] According to another aspect of an exemplary embodiment, there is provided a source driver including: a plurality of buffers, each of the buffers respectively including an amplifier configured to amplify an input signal and an output driver configured to output a driving signal to a data line, wherein the amplifier includes a bias device configured to receive a bias voltage and a first current mirror connected between a first voltage and the bias device, and the first current mirror includes: a first transistor and a second